EUVL for HVM: Progress Update

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Outline

- EUV source and system performance
- EUV/193i complementary patterning
- EUV infrastructure

As of PMJ in April

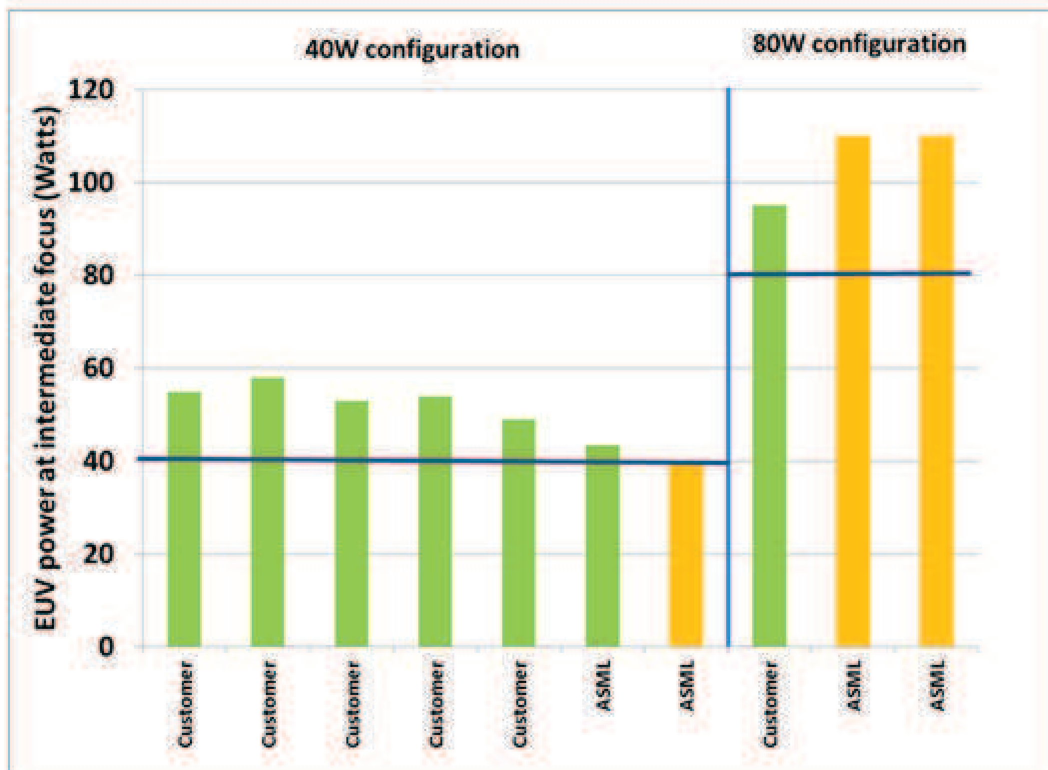
Worldwide fleet 40-80W

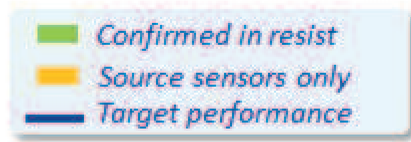
ASML

public
Slide 1

Multiple systems capable of >90W

All systems demonstrated capability to meet performance target



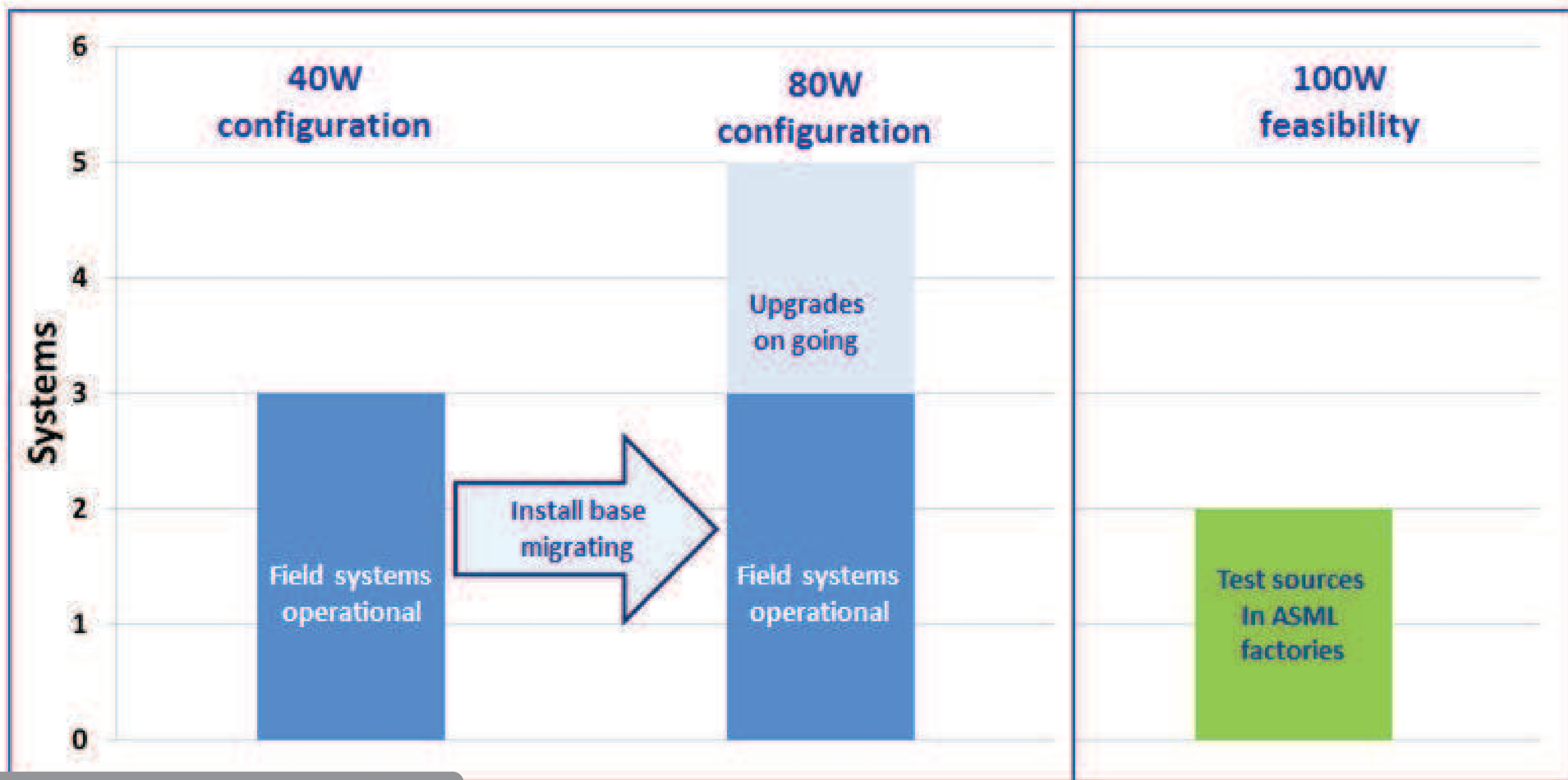


All results normalized to clean collector conditions

Slide courtesy ASML

intel

Install base quickly migrating to 80W config



intel

Short-term productivity >1000wpd

Today: 1,000 wafers per day capability demonstrated

On a field system, using customer exposure conditions, on 2 different days

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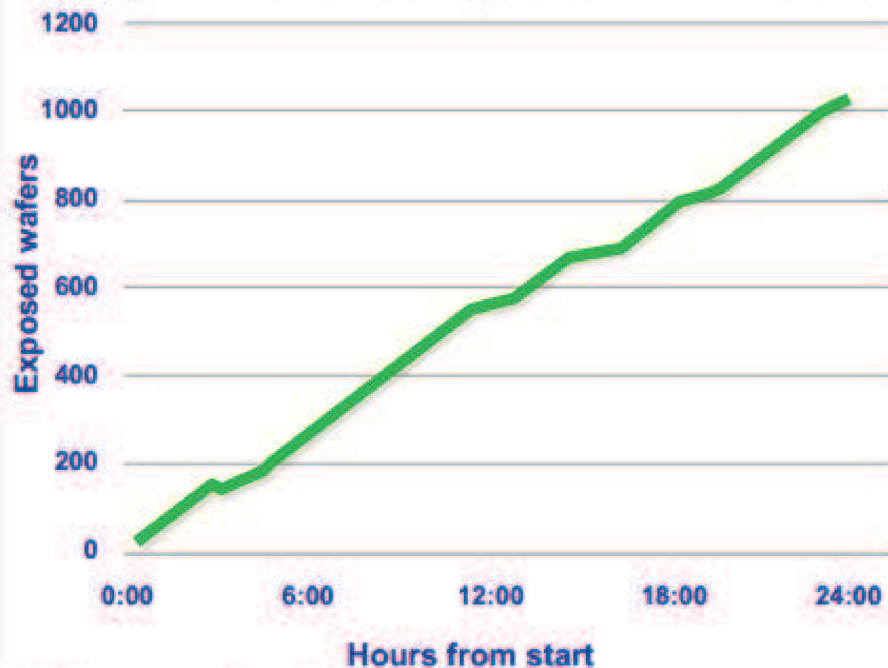
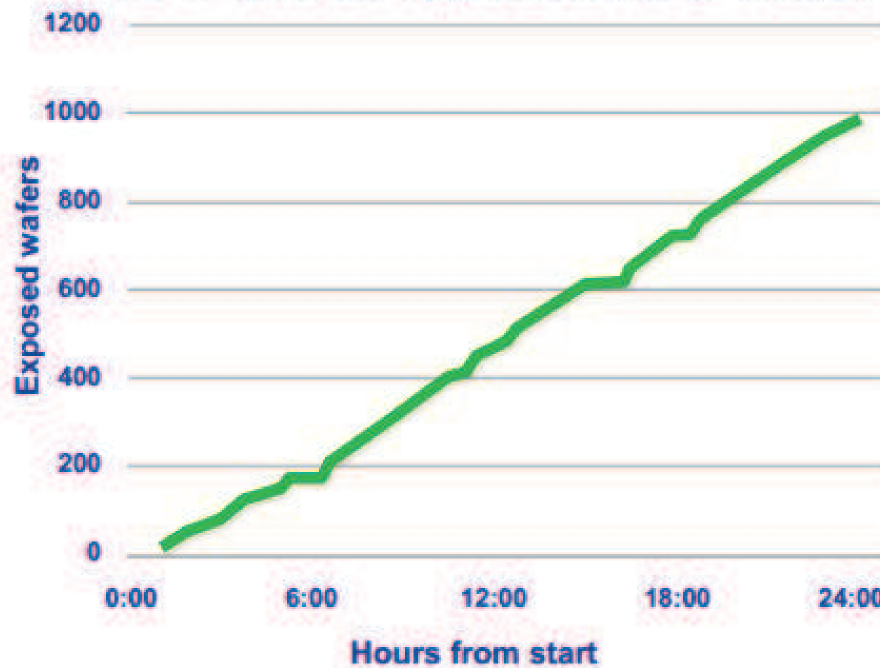
Public
Slide 5
February 2015

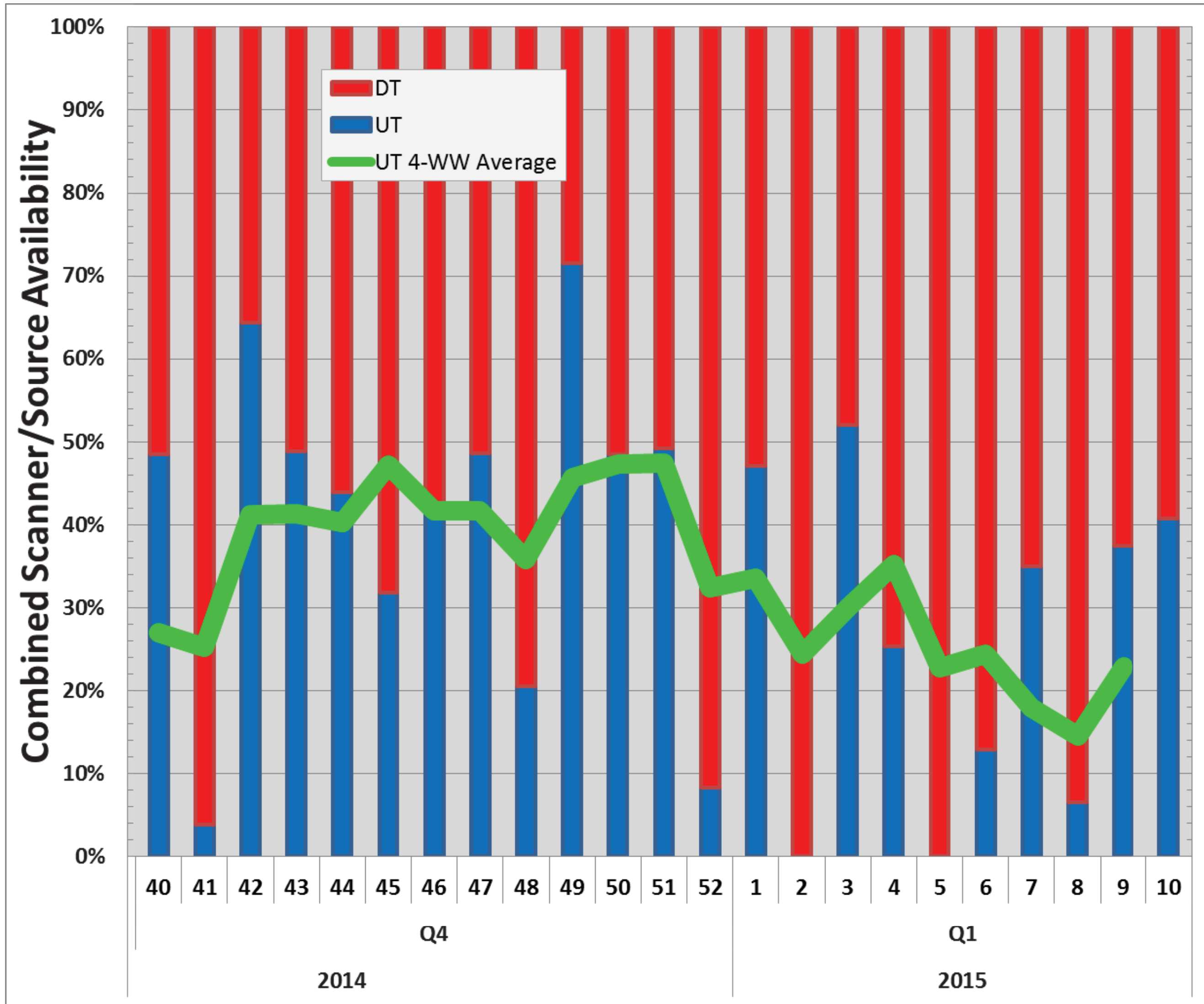




80W source configuration

Alberto Pirati, SPIE Advanced Lithography, 2015

However…



Availability and predictability are still poor

Extended demo of availability and predictability

- 21hrs/day wafer cycling with mix of test-chip wafers (CDs, overlay, in-line defects, e-test) and bare silicon
- 3-hr daily Intel engineering window (no tool work)
- Availability counted 24hrs/day. Wafer output targets set for 21hrs/day in 40W config.
- Only good wafers (meeting dose control specs) counted
- Goal: demonstrate tool can run as advertised for 40W config today, *including imaging and overlay*

Targets and results from 4-week demo

	Nominal Target	Demo-Time Adjusted Target	Result
Availability (scanner + source)	**46%**	**46%**	**61%**
TPT - good wafers per day	**180**	**170**	• **280** normalized WPD • ***260*** actual exposed WPD (raw count)
TPT - good wafers per week	**1260**	**1189**	• **1959** normalized WPW • ***1822*** actual exposed WPW (raw count)
No consecutive DT > 72hrs	**<72hrs**	**<72hrs**	Max consecutive downtime = **36hrs** (DG swap + Sn catch drain + RF generator failure/replacement on PA0)

- Goal: demonstrate tool can run as advertised for 40W config today
- Targets based on 125 fields/wafer at 15mJ/cm^2 dose
- Actual wafers exposed were a variety of shot maps and doses, so "normalized" count converts to equivalent at 125 fields/15mJ
- Integrated test-chip wafers allowed verification of imaging, overay, and defects throughout demo → results all good

Demo cumulative wafers per week

Cummulative Exposed Wafers Per Week
2500
2000
1500
1000
500
0
1 2 3 4 5 6 7 1 2 3 4 5 6 7 1 2 3 4 5 6 7 1 2 3 4 5 6 7
1 2 3 4
Week . Day
Actual Intel
Normalize ATP
Target

Demo in-line defect trend

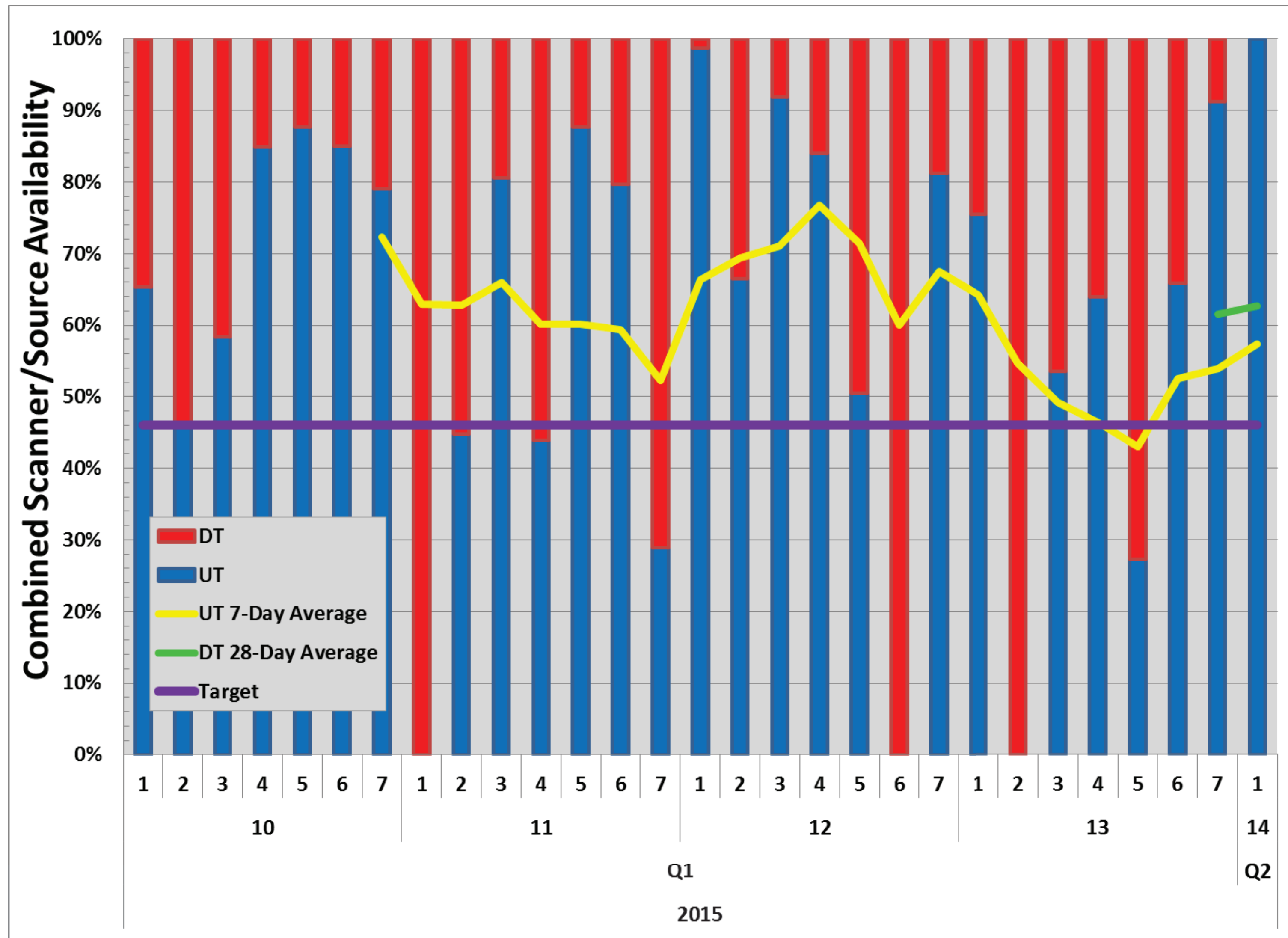
Pattern defects from new track clean up over demo

WW10 WW11 WW12 WW13

Comparable to 193i

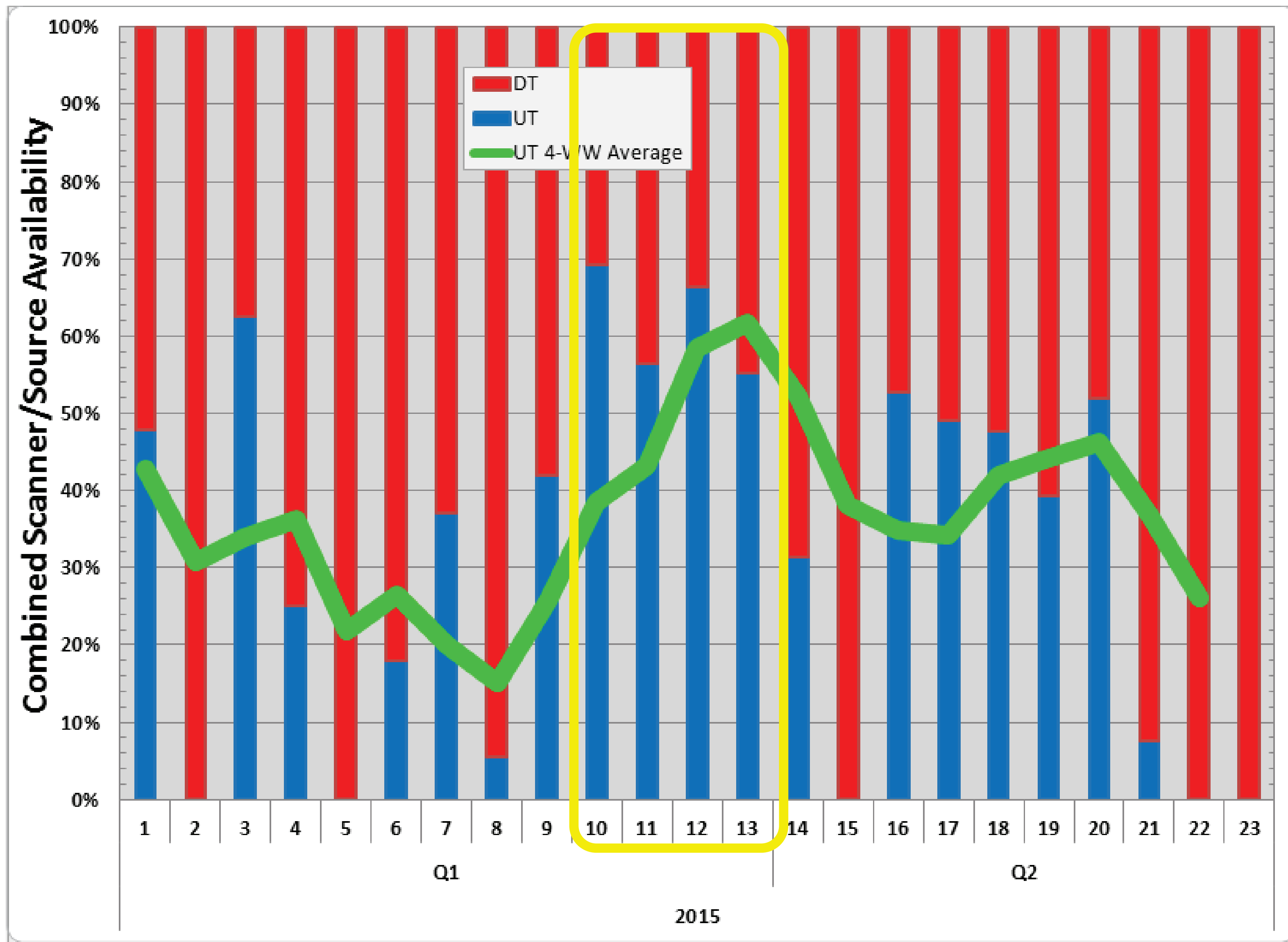
- Track cleans up over time. Scanner contribution is OK.

Demo availability (4 weeks)



- Far from OK for production, but better than expected for current 40W config

Over longer term, availability is unstable



Summary of EUVL status

- Two years of solid progress on EUVL
  - Eight 0.33NA systems shipped, generally meeting all performance specs not related to source power
  - 80W config proliferating quickly, and 100W (@IF) MOPA/PP demonstrated in the field
  - ~500wpd, then ~1000wpd in short-term (1-2 day) demonstrations
  - 4 week demonstration of availability and output consistent with 40W tool configuration, and stable imaging and overlay performance
- Introduction in production is a question of "when" rather than "if"
  - Availability, stability and operating cost are still concerns
  - Need to ensure infrastructure does not gate HVM